UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,853	09/20/2000	Shin-ichiro Tago	FUJH 17.759	5899

26304 7590 02/22/2006

KATTEN MUCHIN ROSENMAN LLP
575 MADISON AVENUE
NEW YORK, NY 10022-2585

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,853	TAGO ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,10 and 11* is/are allowed.

6)☒ Claim(s) *8,9 and 12-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Extension of Time as received on 12/19/2005..

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner recommends incorporating the idea of the multiple buffers and their purposes into the title.

Claim Objections

4. Claim 4 is objected to because of the following informalities: In the 3rd paragraph (first line), insert --a-- before "fourth". Also, in the 4th paragraph, the phrase "branch target address information of further next branching instruction inside said first instruction sequence" is grammatically incorrect. Please reword this phrase in a more clear fashion. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 8-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 8 recites the limitations "said branching instruction" and "the branching instruction." There is insufficient antecedent basis for this limitation in the claim because in claim 6, the applicant refers to both a first and second branching instruction. Applicant cannot claim "said branching instruction" and be referring to two separate instructions. If applicant wants to refer to two separate instructions, then it is suggested that applicant use language along the lines of "both the first and second branching instructions".

8. Claim 9 recites the limitations "said branching instruction". There is insufficient antecedent basis for this limitation in the claim because in claim 6, the applicant refers to both a first and second branching instruction. Furthermore, is "a branching instruction" the same as "said branching instruction? If so, the claim should be modified to be more clear. Applicant cannot claim "said branching instruction" and be referring to two separate instructions. If applicant wants to refer to two separate instructions, then it is suggested that applicant use language along the lines of "both the first and second branching instructions".

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claim 12 is rejected under 35 U.S.C. 102(e) as being anticipated by Asato, U.S. Patent No. 6,289,442 (as applied in the previous Office Action).

11. Referring to claim 12, Asato has taught an information processing device with pipeline processing comprising:

a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branch instruction. See the abstract, Fig.1, and Fig.6B, and note that both a target and sequential side are fetched and tagged. In addition this fetching and tagging occurs despite branch prediction. See column 13, lines 44-62.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1, component 12.

c) a memory bus access portion which accesses said main memory. See Fig.1, component 12, and column 5, lines 12-14.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries. This can also be viewed as a number of sub-buffers.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction for the branching instruction which is stored in said instruction buffer. See Fig.1, component 14.

f) if the branching direction of said branching instruction is not yet determined, said cache controller performs a memory bus access to said main memory according to a branching

direction predicted by the branching prediction portion. See column 13, lines 55-62, and note that when a branch prediction occurs (in this case, assume the branch is predicted not-taken), a block of instructions would be fetched along the sequential path. The fetch address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, would be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asato in view of Lee et al., Instruction Cache Fetch Policies for Speculative Execution, 1995 (as applied in the previous Office Action and herein referred to as Lee).

14. Referring to claim 13, Asato has taught an information processing device as described in claim 12.

a) while the branching direction of said branching instruction is not yet determined, if the cache controller has performed a cache miss with respect to an instruction in the predicted branching direction of said branching instruction, said cache controller performs the memory bus access to the main memory for an instruction fetch. See column 13, lines 55-62, and note that when a

branch prediction occurs (in this case, assume the branch is predicted not-taken), a block of instructions would be fetched along the sequential path. The fetch address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, would be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

b) Asato has not taught that while the branching direction of said branching instruction is not yet determined, if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops said instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if said cache controller has performed a cache miss with respect to an instruction which is not in the predicted branching direction, said cache controller does not perform the memory bus access and stops the instruction fetch.

15. Referring to claim 14, Asato has taught an information processing device as described in claim 12.

a) Asato has not taught that while the branching direction of said branching instruction is not yet determined and the predicted branching direction of said branching instruction is the sequential side, in the event of said cache controller performing a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops said instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if said cache controller has performed a cache miss with respect to said target side instruction, said cache controller does not perform a memory bus access and stops the instruction fetch.

16. Referring to claim 15, Asato has taught an information processing device as described in claim 12. Asato has not taught that while the branching direction of said branching instruction is not yet determined, said cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Consequently, it would have

been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that the cache controller does not perform a memory bus access after a cache miss depending on the predicted branching direction of said branching instruction.

17. Referring to claim 16, Asato has taught an information processing device with pipeline processing, comprising:

a) an instruction fetch portion which fetches both a sequential side instruction sequence and a target side instruction sequence of a branching instruction in spite of a branching prediction of the branching instruction. See the abstract, Fig.1, and Fig.6B, and note that both a target and sequential side are fetched and tagged. In addition this fetching and tagging occurs despite branch prediction. See column 13, lines 44-62.

b) a cache controller which fetches instructions from a cache memory or from a main memory in response to a fetch request from said instruction fetch portion. See Fig.1, component 12.

c) a memory bus access portion which accesses said main memory. See Fig.1, component 12, and column 5, lines 12-14.

d) an instruction buffer which buffers instructions which have been fetched. See Fig.1, components 22A-H (reservation stations). Reservation stations buffer instructions sequences and operands. Also, note instruction cache 16. A cache is essentially a large buffer with many entries.

e) a branching prediction portion which, prior to an execution of a branching instruction, performs a branching prediction of the branching instruction which is stored in said instruction buffer. See Fig.1, component 14.

f) if a branching direction of said branching instruction has been determined and said cache controller performs a cache miss with respect to an instruction in the determined branching direction, said cache controller performs a memory bus access. See column 5, lines 52-54, column 7, lines 38-44, and column 7, lines 11-18. Note that when a branch prediction occurs (in this case, assume the branch is predicted taken), the target address is applied to the instruction cache in order to start fetching the target sequence of instructions. However, if there is a cache miss, slower levels of memory, including main memory, may have to be accessed in order to retrieve the desired instructions, as is known in the art. This is the inherent nature of a memory hierarchy.

g) Asato has not taught that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops said instruction fetch. However, as discussed in column 1 and Table 1 on page 359 of Lee, a "Decode" fetch policy has been taught which only services a cache miss if it is not for a misfetched instruction (i.e., an instruction along the non-predicted path). With such a policy, this misfetched instruction will not be retrieved from main memory (i.e., the fetch is stopped). This prevents bus blocking and cache pollution because no useful cache lines are displaced by erroneous fetches. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Lee into the system of Asato such that if the branching direction of said branching instruction is not yet determined and said cache controller performs a cache miss with respect to an instruction fetch, said cache controller does not perform a memory bus access and stops the instruction fetch.

18. Referring to claim 17, Asato in view of Lee has taught an information processing device as described in claim 16. Asato has further taught that if the branching direction of said branching instruction is not yet determined, an instruction for which a cache hit has been made is prefetched and stored in said instruction buffer. It should be realized that before a branch's direction is determined, instructions along the predicted path will be fetched from memory. If a cache hit occurs, these instructions are brought in from the cache and placed into the instruction buffer (reservation station). See column 13, lines 44-62.

19. Referring to claim 18, Asato in view of Lee has taught an information processing device as described in claim 16. Asato has further taught that instructions are selected from either said instruction sequential side or instruction target side in said instruction buffer depending on the branching direction of the branching prediction portion, and decoded. See column 13, lines 55-62, and note that a not-taken prediction results in fetching of sequential-side instructions.

Allowable Subject Matter

20. Claims 1-7 and 10-11 are allowed.

Response to Arguments

21. Applicant's arguments filed on December 19, 2005, have been fully considered but they are not persuasive.

22. Applicant argues the novelty/rejection of claims 12 and 16 on page 19 of the remarks, in substance that:

> "The cited section [of Asato] does not appear to address the distinct situation in which the branching direction of the branching instruction is not yet determined...the cited section indicates that the next block instruction subsequent to the first branch of instructions is indicated. However,

> this does not appear to disclose or suggest a cache memory accessing a memory based on the branching direction predicted by the branching prediction portion."

23. These arguments are not found persuasive for the following reasons:

a) Regarding claim 12, the point of this passage was to show that in response to a branch prediction (the actual branching direction is not yet determined), certain instructions are fetched. For instance, if a branch is predicted not-taken, then the instruction immediately following the branch is fetched. This instruction will be fetched from instruction cache 16 (Fig. 1) if the instruction exists in the cache. However, if a cache miss occurs (i.e., the instruction is not in the cache), then it is inherent that main memory will be accessed to fetch the instruction unless the system is told otherwise. The examiner asserts that applicant is essentially claiming a memory hierarchy. In a memory hierarchy, the processor tries to fetch instructions/data from the fastest memory first, and if the instructions/data are not in the fastest memory, then the processor tries at the next fastest memory, and so on, until it is found.

b) A similar argument applies to claim 16, except that in the rejection of claim 16, a secondary reference was used to tell the system otherwise. That is, the system is told not to look at the next fastest memory for the instructions/data since the branching direction is not yet determined.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Jager, U.S. Patent No. 5,423,048 has taught a system in which a tree is built having branches representing branch path instruction sequences. Each node in the tree represents a branch instruction and the two branches emanating from the node represent the fall-through and sequential paths. Multiple paths are fetched and the incorrect paths are invalidated.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
February 14, 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100